I Sem VLSI Design & Embedded Systems

USN | | | | | | | | | | |

12EC130

M.Tech. Degree Examination, February 2013
VLSI Design Verification

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions.*
2. State design examples wherever relevant.

1 a. Explain verification as a reconvergent model. What is the effect of 'human factor' in verification? How do you address it? **(10 Marks)**

b. Discuss the need of verification in 30C design context. Address various challenges of verification of VLSI designs. **(10 Marks)**

2 a. State atleast three ways to reduce verification time. What is a test bench? Explain different components of test bench. **(10 Marks)**

b. Discuss various co-simulation options in VLSI design verification. Mention different tools required for verification. **(10 Marks)**

3 a. Explain the following in the context of verification:
i) Verification intellectual property ii) Hardware modellers. **(10 Marks)**

b. Explain with a design case, the following:
i) Different coverages ii) Different metrics **(10 Marks)**

4 a. How sould we decide on the level of verification (unit level, board level etc.)? **(04 Marks)**

b. Define 'first time success' in context of VLSI design. Discuss the contents of verification plan. **(06 Marks)**

c. Explain the following terms:
i) Directed test ii) Random test
iii) Constrained random test iv) Coverage driven random test. **(10 Marks)**

5 a. What are the two types of timing analysis used in VLSI design verification? Compare them in terms of coverage, accuracy and usage. **(05 Marks)**

b. What do you need to perform STV on the VLSI design verification? **(05 Marks)**

c. Explain STV methodology of timing analysis of VLSI Design. **(10 Marks)**

6 a. Define terms:
i) Slew of a waveform ii) Skew of clock iii) Critical path
iv) False path v) Multicycle path. **(10 Marks)**

b. Which are the four types of timing paths in any VLSI Design? How is path delay computed in pre-layout design and post layout design? **(10 Marks)**

7 a. i) Mention various methods of representing a Boolean function. Explain their merits and demerits. **(06 Marks)**
ii) Generate BDD for function $F = x1.\ x2 \vee x3$. **(04 Marks)**

b. What is SAT? Explain with an example the basic SAT algorithm. **(10 Marks)**

8 Write technical notes on following:
a. Verification IP and reuse b. Equivalence checking
c. Cross talk glitch analysis d. Verification plan
e. Linting **(20 Marks)**

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